

Functional Plastic Liquid Crystal Displays from II-VI Semiconductor Nanocomposite Thin Film Transistors on Polymers

F. MacNab*, P. Frechette*, B. Fong*, T. Li,*

I. Shih**, W. Schambach**, and M.P. Andrews**

*Silk Displays, 424 Guy St, Montreal, Quebec, H3J 1S6, Canada bfong@silkdisplays.com

**McGill University, Montreal, Quebec, H3A 2K6, Canada, mark.andrews@mcgill.ca

ABSTRACT

We describe a low temperature II-VI semiconductor chemical bath deposition process to create semiconductor-on-plastic (SoP) thin film transistors derived from nanocrystalline CdS composite thin films on “smart plastic” substrates for use in liquid crystal displays. Nanocrystalline CdS was deposited by chemical bath deposition onto aluminum oxide gate dielectric. The current-voltage characteristics were typical of normal field effect transistors. Mobilities on the order of $0.34 \text{ cm}^2/\text{V}$ were obtained, with a small threshold of -0.75 V , implicating acceptor levels at the interface of the dielectric and semiconductor. The CBD method was extended from 1-inch to 5-inch diagonal TFT arrays, suggesting a pathway to scalable TFT fabrication over large area plastic substrates. The TFT substrate was assembled into a display format with RGB LED backlights to achieve color mixing at video frame speeds.

Keywords: SoP, plastic display, nanocomposite display, smart plastic, nanocrystalline semiconductor

1 BACKGROUND

It has been widely argued that the development of low cost, plastic displays will lead to dramatic increases in the variety and utility of consumer, industrial, transportation and military display products. Moreover, the appealing feature of flexibility of plastics may stimulate creation of entirely new display markets. The primary advantages of plastic substrates with respect to glass are weight reduction, flexibility, and resistance to display breakage during fabrication and use. In addition, appropriate plastic substrates may cost significantly less than glass substrates currently used in displays. Figure 1 shows an assembled 5-inch diagonal TFT LCD screen that we have fabricated on “smart plastic” (see below) at Silk Displays. Plastics are also appealing substrates for the development of large area displays, such as those used in advertising and simulators. They are also attractive from the perspective of volume display production via roll-to-roll manufacturing. Nevertheless, plastics pose significant challenges to the fabrication of TFTs via standard semiconductor processes. One challenge arises from the fact that plastics have a ceiling processing temperature which is well below that of conventional silicon processing. Secondly, the thermo-mechanical properties of polymers are radically different

from those of the guest inorganic materials that make up the resident TFTs. Differences in thermo-mechanical properties frequently result in TFT, gate and data line failures. Broadly then, the desirable feature of flexibility also makes semiconductor on plastics (SoP) quite difficult to realize. To date, researchers have sought to circumvent this limitation by depositing amorphous silicon ($a\text{-Si:H}$) at reduced temperatures [1], or by recrystallization of polysilicon with pulsed lasers [2,3]. Nevertheless, it is sur-

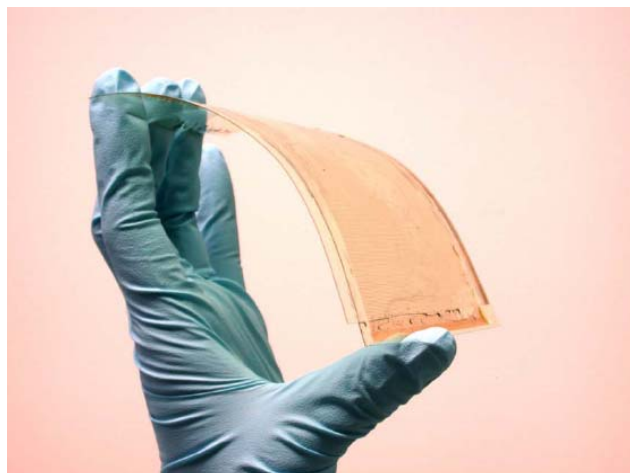


Figure 1: Assembled active matrix “smart plastic” LCD display element prior to integration with RGB backlights. The laminate is approximately 0.4 mm thick

prising that there is little published research that focuses on modifying the plastic substrate in combination with low temperature strategies for SoP. To address this, we have adopted what we call a “smart plastic” approach combined with a low temperature chemical bath deposition to build TFTs on compliant substrates. The “smart plastic” substrate is thermally and chemically conditioned to have a shape memory (dimensional reversibility) built into it together with a (“smart”) capacity to adapt to various semiconductor-like fabrication steps. (Moreover, the substrate in combination with functional layers (electronics, liquid crystal, and others) suggests a broader range of applications for plastics with embedded intelligence.)

As an alternative to the use of silicon for SoP, we have explored chemical bath deposition (CBD) of CdS and CdSe to create the semiconductor element in the TFT [4]. Research into the synthesis of binary metal chalcogenides of $A^{II}B^{VI}$ semiconductors in nanocrystalline form by

chemical bath deposition (CBD) has rapidly evolved in recent times. CBD is a generic term given to the kinetically controlled deposition of solid films from solution, typically without changing the oxidation state of the metal deposited [4]. Its appeal for display technologies is the apparent simplicity of the liquid phase coating process, suggesting scalability from small to very large area substrates. In the experiments described below, we use a successive ionic layer adsorption and reaction method to deposit nanocrystalline CdS films to create field effect devices on smart plastics. These devices are shown to switch pixels containing vertically aligned liquid crystal at speeds commensurate with the demands of field sequential color technology. We use red, blue and green light emitting diodes to achieve color mixing in the time domain, with one third the number of transistors and no color filter, as compared with conventional LCD constructs.

2 EXPERIMENTAL

For our experiments we used 200 μm thick films of a custom-formulated polyarylester compound. The polymer was treated in a series of steps in order to obtain a substrate with a shape memory sufficient to allow excellent multilevel mask registration to create TFTs, data and gate lines. Pre-treatment of the plastic film allowed temperature excursions as high as 220 $^{\circ}\text{C}$ during the course of the semiconductor fabrication process. The TFT architecture is shown in Figure 2.

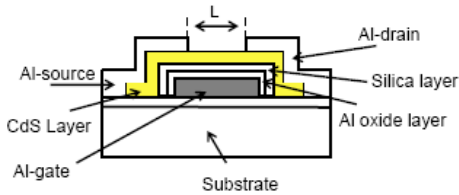


Figure 2: TFT architecture

It consists of an aluminum gate, aluminum oxide dielectric layer, PECVD silicon oxynitride, a II-VI semiconductor and aluminum source and drain electrodes. Processing was done in part in the Nanotools Facility of McGill University and in the clean room of Silk Displays. Aluminum was deposited on the plasma roughened substrate by sputter deposition. Films on the order of 0.75 μm were subsequently patterned by photolithography and wet etched to create the gate lines. The gate region was quantitatively anodized at neutral pH. Annealing of this gate dielectric gave isolation layers with breakdown voltages on the order of 8 MV/cm. Capacitance measurements revealed a dielectric constant of ~ 9 for the annealed anodized oxide. Leakage currents were on the order of 10^{-10} A. CdS was chosen to prototype the initial experiments, despite the lower mobilities compared with CdSe. CdS films were formed at 70 $^{\circ}\text{C}$ by reaction of thiourea, ammonia (complexant) and CdCl_2 . Pixel electrodes were fabricated from gold films or from ITO. Liquid crystal material was

vertically aligned with a polyimide alignment layer. The LC was sandwiched between the lower (TFT equipped) plastic substrate and the upper plastic layer coated with ITO. Plastic spacers were used to maintain a uniform cell gap. Color switching under the control of off-board electronics was achieved by flashing side illuminating red, blue and green light emitting diodes. Figure 3 shows an optical micrograph of a section of smart plastic supporting pixels and their associated TFTs.

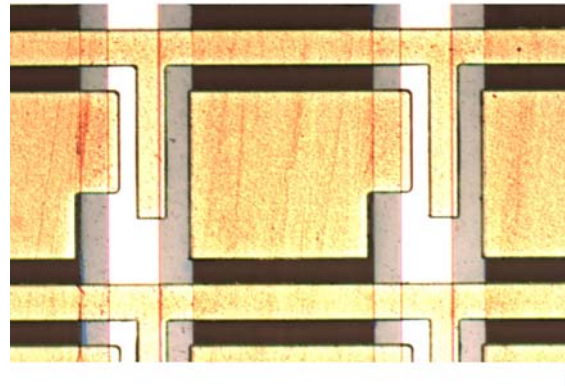
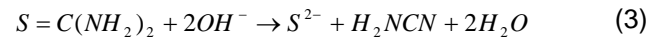
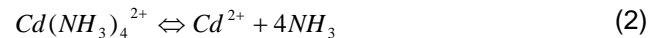
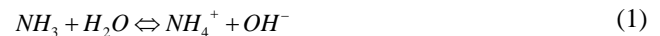


Figure 3: TFT array elements on “smart plastic” substrate.

3 RESULTS AND DISCUSSION

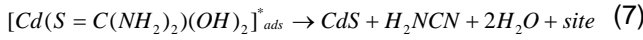
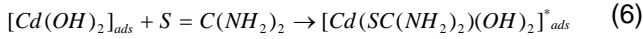
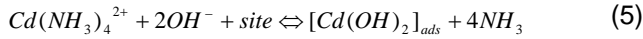
3.1 II-VI Films by CBD

TFT device performance depends strongly on the manner in which the II-VI semiconductor layer is deposited. In the discussion that follows, we focus on CdS. Four primary reactions govern the solution phase behavior in the thiourea/ammonia system:



The concentration of metal ions, chalcogenide sources, complexant (NH_3) and hydroxide ions determines the rate of CdS formation and whether the semiconductor forms as a film or as particles dispersed in the reaction solution. Films that are created mainly by particle deposition from solution suffer several drawbacks. In the first place, the films adhere poorly and secondly, they consist of aggregates of particles showing ranges of quantum size effects, much like those of semiconductor particles produced by well known sol ripening techniques in solution. In the past, three-dimensional quantum-size effects have been observed from chemically deposited CdSe films [5], so care must be taken at this step to confer

reproducible electronic properties on the film. The morphology of deposited films also depends highly on the initial reagent concentrations because these determine whether the film will grow by an ion-by-ion process, by the aggregation of colloidal particles from solution on the surface of the substrate, or by a combination of the two mechanisms. Successive ionic layer adsorption and reaction is thought to proceed by the following mechanism:



CdS will form on the surface by an ion layer process only in the presence of Cd(OH)₂, with the concentration of the latter complex depending strongly on solution pH. In practice, it is difficult to ensure that films are deposited exclusively by the ion accretion method. This is because the equilibrium concentration of free Cd²⁺ does not remain constant as required by the ion-ion accretion model. In the end, the nanocomposite is thought to be deposited by a mixture of ion-ion and particle deposition processes. Film growth can be described then in terms of three phases. The first phase involves the creation of Cd(OH)₂ on the substrate film surface. This is followed by a short nucleation step to create nanoscale CdS grains, and then by coalescence. CdS crystals, typically around 4 nm incorporated from solution, are much smaller than film grown grains. Grains of CdS microcrystals nucleated on the film can be as large as 140 nm depending on the deposition conditions [6]. CBD deposited films are often non-stoichiometric by as much as 2%. In our experiments, the CBD conditions resulted in a slight excess of Cd in the CdS films. Films with incorporated solution grown grains have many more grain boundaries than films without. This can have a large influence on the transport properties of the CdS semiconductor. CdS films deposited by the ion-by-ion mechanism exhibit lattice orientation perpendicular to the substrate. Studies of the crystal structures of deposited CdS films variously reveal hexagonal close packing, cubic, or mixture of the two. Stacking faults seem to be responsible for the change from hexagonal to cubic structure during depositions. Electron micrographs of dense films in cross section show grain structures that evolve as “towers” of oriented crystals. These features result from the coalescence of islands where nucleation originates. The grains then continue to grow upward in a highly oriented fashion. Interestingly, visual evidence suggests that even after coalescence the grain boundaries between islands are maintained at the interface as the towers grow.

As the number of grain boundaries increases, the mobility of the charge carriers in the film decreases and the number of intrinsic charge carriers increases. Overall, one can obtain polycrystalline films containing nanocrystalline regions with a large number of grain boundary interfaces. We found these interfaces to be quite metastable with respect to temperature so that short annealing times at 250

°C could be used to improve the I-V characteristics of the devices. Annealing greatly improves the properties of the CdS by two mechanisms. Firstly, the high surface energies of the nanocrystalline grains allows adjacent particles to combine into larger particles upon heating, reducing the number of grain boundaries in the film. Secondly, when annealing is conducted in air, oxygen converts excess cadmium in the film to CdO. The CdO reduces the number of intrinsic charge carriers in the semiconductor.

3.2 Electrical Characteristics

Test structures were fabricated on the plastic substrate to systematically evaluate key process parameters required to build a functional plastic LCD from the nanocrystalline CBD CdS. A typical test structure is shown in Figure 4.

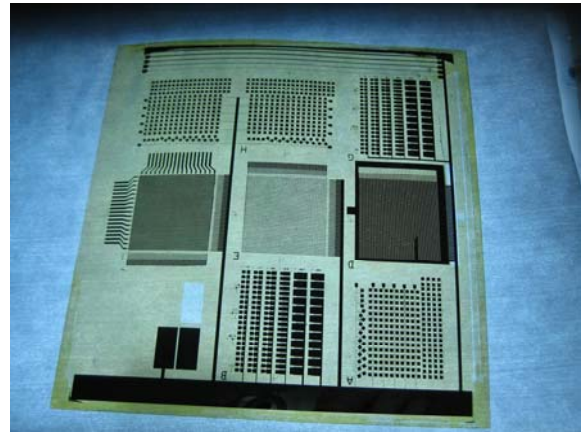


Figure 4: Test structure device array on 5-inch diagonal plastic substrate.

Dark drain current (I_d)-drain voltage (V_d) characteristics of the TFTs fabricated by CBD are shown for different positive gate voltages V_g in Figure 5. No attempt was made to optimize the I-V characteristics in these samples. It is

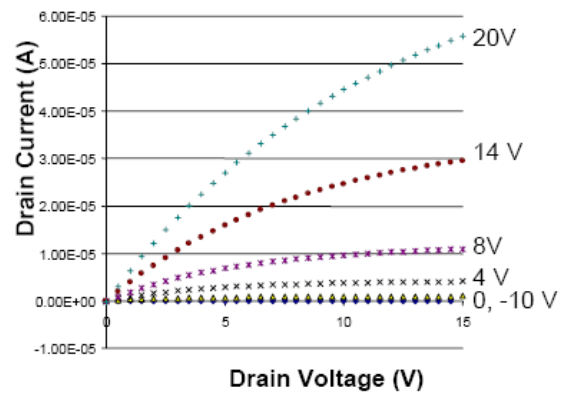


Figure 5: Dark current-dark voltage characteristics for different values of gate voltages for nanocrystalline CdS TFTs.

evident that normal field effect transistor characteristics are obtained in the case of positive V_d . The current saturates at a certain V_d depending on the gate voltage. The on/off ratio is better than 10^5 . We measured the channel widths and lengths with a probe station. The transistor mobility of CdS was found to be $0.34 \text{ cm}^2/\text{V}$. A small negative threshold voltage of -0.7 V suggests the presence of acceptor levels at the interface of the dielectric and the semiconductor.

3.4 Display Switching

The TFT array was subsequently integrated into a $400 \mu\text{m}$ thick plastic LCD (Figure 1). The bottom substrate was coated with a polyimide orientation layer and then the one-drop-fill method was used to incorporate a vertically aligned liquid crystal medium. Cell gaps were adjusted to minimize the threshold for switching the liquid crystal. Color mixing was achieved by flashing red, blue and green light emitting diodes comprising the back light. We used off-board electronics to control the LEDs and the TFTs. For clarity, Figure 6 shows columns and rows of red and green pixels illuminated separately in one section of the display.

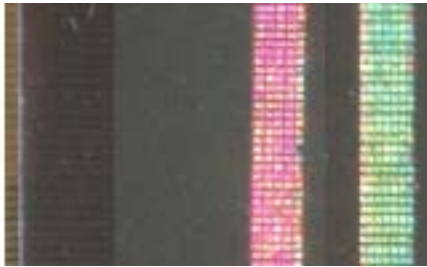


Figure 6: Stripes of pixels showing red and green from the light emitting diode backlights in an implementation of the nanocrystalline CdS smart plastic LCD.

4 ACKNOWLEDGMENTS

We gratefully acknowledge the assistance of Vito Logiudice, manager of the McGill Nanotools Facility for assistance in the early stages of this work. Technical work was supported in part by a service agreement between McGill University and Silk Displays.

REFERENCES

- [1] A. Sazonov, D. Stryahilev, and A. Nathan, Proc. 3rd Int. Conf. Microelec. (MIEL 2002), 2, 525, 2002.
- [2] P.G. Carey, P.M. Smith, S.D. Theiss, and P. Wickboldt, J. Vac. Sci. Technol. A17, 1946, 1999.
- [3] T. Naguchi, J. Y. Kwon, J.S. Jung, J. M. Kim, K. B. Park, H. Lim, D. Y. Kim, H. S. Cho, H. X. Yin and W. Xianyu, Japan J. Appl. Phys., 45, 4321, 2006.

- [4] E. Penia, L. Pentilie, T. Botila, J. Optoelectron. Adv. Mater., 2, 593, 2000; also F. Gan and I. Shih, F.Y. Gan and I. Shih, J. Vac. Sci. Technol. A, 20, 1365, 2002; F.Y. Gan and I. Shih, IEEE Trans. Electron Dev., 44, 15, 2002.
- [5] G. Hodes, A. Albu-Yaron, F. Decker, and P. Motsiuke, Phys. Rev. B 36, 4215, 1987.
- [6] Rusu, M., Rumberg, A., Schuler, S., J. Phys. Chem. Solids, 64, 1849, 2003.